IN THE SPECIFICATION:

Paragraph beginning at line 2 of page 8 has been amended as follows:

Also, if a plurality of image sensor ICs each having a photoelectric converter and a signal processing circuit formed on one semiconductor substrate are mounted, and reference voltages to be supplied to the respective image sensor ICs are made common, then it is possible to reduce a dark output difference in level, among chips, of output signals of all the image sensor ICs.

Paragraph beginning at line 10 of page 10 has been amended as follows:

In addition, according to another aspect of the present invention, there is provided an image sensor IC including: a plurality of photodiodes serving as a plurality of photoelectric ~~converter~~ converters; and a plurality of reset switches connected to the plurality of photoelectric ~~converter~~ converters for initializing the plurality of photoelectric ~~converter~~ converters, respectively, wherein one terminal of each of the plurality of reset switches are electrically connected to a reference voltage terminal.

Heading beginning at line 10 of page 14 has been amended as follows:

~~DESCRIPTION OF THE PREFERRED EMBODIMENTS~~ DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Paragraph beginning at line 16 of page 15 has been amended as follows:

FIG. 2 is a circuit diagram of a sample/hold circuit according to the first embodiment of the present invention. This sample/hold circuit shown in FIG. 2 can be used as the sample/hold circuit 21 and the sample/hold circuit 27. This sample/hold circuit includes a transmission gate 30, a dummy switch 31, and a capacitor C1. In this sample/hold circuit, in order to cancel a noise of a pulse signal ~~ÖSH~~ ϕSH and a noise of a pulse signal ~~ÖSHX~~ ϕSHX as an inverted pulse signal of the pulse signal ~~ÖSH~~ ϕSH with each other, an NMOS and a PMOS of the transmission gate 30 are made identical in transistor size to each other, and a gate area of transistors of an NMOS and a PMOS of the dummy switch 31 is made half a gate area of the transistors of the transmission gate.

Paragraph beginning at line 5 of page 17 has been amended as follows:

FIG. 6 is a circuit diagram of a voltage clamp circuit according to the first embodiment of the present invention. This voltage clamp circuit shown in FIG. 6 can be

used as the voltage clamp circuit 25. This voltage clamp circuit includes a transmission gate 30, a dummy switch 31, and a capacitor 33. In this voltage clamp circuit, in order to cancel a noise of a pulse signal ~~ÖCLAMP~~ ϕCLAMP and a noise of a pulse signal ~~ÖCLAMPX~~ ϕCLAMPX as an inverted pulse signal of the pulse signal ~~ÖSH~~ ϕSH with each other, an NMOS and a PMOS of the transmission gate 30 are made identical in transistor size to each other, and a gate area of transistors of an NMOS and a PMOS of the dummy switch 31 is made half a gate area of the transistors of the transmission gate.

Paragraph beginning at line 10 of page 18 has been amended as follows:

The amplification unit 3 may be constituted by a MOS source follower, a voltage follower amplifier, or the like, and may also be provided with an amplifier enable terminal 10 for selection of an operation state. In addition, a parasitic capacity 9 exists between a gate and a source of the MOS transistor 6. Also, a second current source 51 is connected to the source of the MOS transistor 6. This second current source 51 is turned ON and turned OFF in accordance with an enable signal ~~ÖRR~~ ϕRR. Then, in a turn-ON state, substantially the same current as that of the first current source 8 is caused to flow through the second current source 51.

Paragraph beginning at line 8 of page 19 has been amended as follows:

At the time when the reset switch 2 is turned ON in accordance with ~~ÖR(n)~~ φR(n), a voltage appearing at an output terminal Vdi of the photodiode 1 is fixed to a reference voltage Vreset. On the other hand, at the time when the reset switch 2 is turned OFF, the voltage appearing at the output terminal Vdi takes a value which is obtained by adding an off-noise to the reference voltage Vreset. This off-noise becomes a random noise since an electric potential fluctuates whenever the reset is carried out. Consequently, in order to prevent the random noise from being generated, a difference between the output voltage of the amplifier 3 after the reset, and the output voltage of the amplifier 3 after the subsequent storage of photocharges in the photodiode is taken.

Paragraph beginning at line 20 of page 19 has been amended as follows:

Then, as shown in FIG. 9, after the reset switch 2 is turned OFF in accordance with ~~ÖR(n)~~ φR(n), the transfer switch 4 is turned ON in accordance with ~~ÖT1(n)~~ φT1(n) to read out the reference signal to the capacitor 5 for a time interval TR. At this time, the second current source 51 is turned ON in accordance with an enable signal ~~ÖRR(n)~~ φRR(n), whereby a source electric potential of the MOS transistor 6 is made substantially the same as that in a read operation while

~~ÖSCH(n)~~ φSCH(n) is held in a turn-ON state. The reference signal is held in the capacitor 5 for one time interval. For this time interval, the photocharges are accumulated in the photodiode 1, and hence the electric potential appearing at the terminal Vdi fluctuates in correspondence to a quantity of photocharges. At the time when the channel selection switch 7 is turned ON in accordance with ~~ÖSCH(n)~~ φSCH(n) of the next time interval, for a time interval REF, the reference signal held in the capacitor 5 is read out to the common signal line 11. Next, at the time when ~~ÖT1(n)~~ φT1(n) is turned ON to read out an optical signal to the capacitor 5, this optical signal is read out to the common signal line 11. At this time, the second current source 51 is turned OFF. This causes the source electric potential of the MOS transistor 6 when the reference signal is read out to the capacitor 5 for a time interval TR, and the source electric potential of the MOS transistor 6 when the optical signal corresponding to a quantity of electric charges accumulated in the photodiode is read out to the capacitor 5 for a time interval TS to be substantially identical to each other. Consequently, it is possible to reduce an influence of the parasitic capacity 9 on the electric charges accumulated in the capacitor 5. As a result, it is possible to reduce an offset of the dark output voltage.

Paragraph beginning at line 24 of page 20 has been amended as follows:

From the above-mentioned operation, if there is taken a difference between an output voltage VOUT on the common signal line 11 for a time interval REF of ~~ÖSCH(n)~~ φSCH(n), and an output voltage VOUT on the common signal line 11 for a time interval SIG of ~~ÖSCH(n)~~ φSCH(n), then it is possible to remove the fixed pattern noise and the random noise caused by the reset switch 2. Next, after ~~ÖTI(n)~~ φTI(n) is turned OFF, ~~ÖSCH(n)~~ φSCH(n) is turned OFF, and ~~ÖR(n)~~ φR(n) is turned ON to carry out the next reset of the photodiode. Then, ~~ÖTI(n)~~ φTI(n) is turned ON again to read out the reference signal to the capacitor 5 for the time interval TR.

Paragraph beginning at line 10 of page 21 has been amended as follows:

After ~~ÖSCH(n)~~ φSCH(n) is turned OFF, the channel selection switch 7 of the next bit is turned ON in accordance with ~~ÖSCH(n+1)~~ φSCH(n+1) to start an operation for reading out a reference signal of the next bit. All other pulses of an (n+1)-th bit are shifted backwardly from the pulses of the n-th bit by a time interval when ~~ÖSCH~~ φSCH is held in a turn-ON state.

Paragraph beginning at line 16 of page 21 has been amended as follows:

In the above description, the second current source 51 may be removed. In this case, the enable pulse signal ~~ÖRR~~ $\underline{\phi RR}$ becomes unnecessary accordingly.

Paragraph beginning at line 5 of page 22 has been amended as follows:

An output signal outputted through the output terminal VOUT is inputted to the input terminal VIN. A sample/hold pulse signal ~~ÖSH1~~ $\underline{\phi SH1}$ is turned ON when the reference signal begins to be read-out, and is turned OFF before reading out of the reference signal ends. As a result, the reference signal is sampled and held. The signal at the input terminal VIN and the sampled and held signal are inputted to the subtracter. For the time interval of the first half, the reference signals identical to each other are inputted to the subtracter, and for the time interval of the second half, the reference signal which has been sampled and held and the optical signal are inputted to the subtracter. Thus,an output signal of the subtracter, for the time interval of the first half, is at a level VREF and for the time interval of the second half, is at a level which is obtained by adding t.he level VREF to a level obtained by amplifying a difference between the reference signal and the optical signal gain times. In addition, offsets of the buffer amplifiers 22

and 23, and the subtracter 24 are contained in the output signal for the time interval of the first half, and offsets of the buffer amplifiers 22 and 23, and the subtracter 24, and an offset of the sample/hold circuit 21 are contained in the output signal for the time interval of the second half.

Paragraph beginning at line 2 of page 23 has been amended as follows:

A clamp pulse signal ~~ÖCLAMP~~ ϕCLAMP is added so as to be turned ON before the sample/hold pulse signal ~~ÖSH1~~ ϕSH1 is turned ON and to be turned OFF before the sample/hold pulse signal ~~ÖSH1~~ ϕSH1 is turned OFF. As a result, for the time interval of the first half, an output signal of the voltage clamp circuit 25 is clamped to the level VREF, and for the time interval of the second half, is at a level which is obtained by adding the level VREF to a level obtained by subtracting the output signal of the subtracter for the time interval of the first half from the output signal of the subtracter for the time interval of the second half. As a result, offsets of the buffer amplifiers 22 and 23, and the subtracter 24 are not contained in the output signal of the voltage clamp circuit for the time interval of the second half. In addition, an offset of the sample/hold circuit 21 is small because the circuit is configured such that a noise of the sample/hold pulse signal ~~ÖSH~~ ϕSH and a noise of the pulse signal ~~ÖSHX~~ ϕSHX as an inverted pulse signal of the

sample/hold pulse signal ~~ÖSH~~ φSH cancel each other. From the above, the output signal of the voltage clamp circuit for the time interval of the second half is at a level obtained by adding a level which is obtained by amplifying a difference between the reference signal and the optical signal gain times with the level VREF as a reference.

Paragraph beginning at line 23 of page 23 has been amended as follows:

A sample/hold pulse signal ~~ÖSH2~~ φSH2 is turned ON before and after the optical signal begins to be read-out, and is turned OFF before reading out of the optical signal ends. As a result, the output signal for the time interval of the second half of the clamped output signal is sampled, and is then held for the time interval of the first half of the next bit. Consequently, it is possible to maintain the output level for a long time interval.

Paragraph beginning at line 16 of page 25 has been amended as follows:

~~ÖR, ÖRIN, ÖSIN, and ÖSEL~~ φR, φRIN, φSIN, and φSEL of FIG. 11 simultaneously operate for all bits. Since operation timings of ~~ÖS0, ÖR0, and ÖSCH~~ φS0, φR0, φSCH vary depending on bits, ~~ÖSO, ÖR0, and ÖSCH~~ φS0, φR0, and φSCH are denoted in the form of addition of "(n)".

Paragraph beginning at line 22 of page 25 has been amended as follows:

First of all, an operation of a photoelectric conversion block of an n-th bit will hereinafter be described. The transfer switch 15 is turned ON in accordance with a pulse SI of ~~ÖSIN~~ ϕSIN to read out the optical signal obtained by storing electric charges generated due to incidence of light to the photo diode 1 to the capacitor 13. Next, at the time when the reset switch 2 is turned ON in accordance with a pulse R2 of ~~ÖR~~ ϕR, an output voltage appearing at an output terminal Vdi of the photodiode 1 is fixed to a reference voltage Vreset. On the other hand, at the time when the reset switch 2 is turned OFF, the output voltage appearing at the output terminal Vdi takes a value which is obtained by adding an off-noise to the reference voltage Vreset. Next, right after the reset switch 2 is turned OFF, the transfer switch 14 is turned ON in accordance with a pulse R2 of ~~ÖRIN~~ ϕRIN to read out the reference signal after reset of the photodiode 1 to the capacitor 12. Thereafter, the photocharges are accumulated in the photodiode 1, and hence the electric potential appearing at the output terminal Vdi fluctuates in correspondence to a quantity of photocharges. Since a time interval for the storage ranges from a time point at which reading out of the pulse R2 of ~~ÖR~~ ϕR ends up to a time point at which reading out of the pulse S2 of ~~ÖSIN~~ ϕSIN of the next

time interval ends, this time interval for the storage corresponds to a time interval TS2 shown in FIG. 11. Thus, this time interval for the storage is held for all bits.

Paragraph beginning at line 23 of page 26 has been amended as follows:

During the time interval TS2 for the storage shown in FIG. 11, if the transfer switch 17 is turned ON in accordance with a pulse of ~~ÖS0(n)~~ ϕS0(n), at the same time as the channel selection switch 7 is turned ON in accordance with a pulse of ~~ÖSCH(n)~~ ϕSCH(n), then an optical signal held in the capacitor 13 is read out to the common signal line 11. This time interval corresponds to a pulse width of the pulse S1 of ~~ÖSCH(n)~~ ϕSCH(n). This optical signal is a signal accumulated for a time interval TS1. Next, at the time when the transfer switch 16 is turned ON in accordance with a pulse of ~~ÖR0(n)~~ ϕR0(n), a reference signal held in the capacitor 12 is read out to the common signal line 11. This reference signal is a signal which is reset in accordance with the pulse R2 of ~~ÖR~~ ϕR.

Paragraph beginning at line 11 of page 27 has been amended as follows:

Next, if a channel selection switch 7 of the next bit is turned ON in accordance with ~~ÖSCH(n+1)~~ ϕSCH(n+1), and a transfer switch 17 of the next bit is turned ON in accordance

with a pulse of ~~ÖS0(n+1)~~ φS0(n+1) after ~~ÖSCH(n)~~ φSCH(n) is turned OFF, then an operation for reading out an optical signal of the next bit is started. All other pulses of an (n+1)-th bit are shifted backwardly from the pulses of the n-th bit by a time interval when ~~ÖSCH~~ φSCH is held in a turn-ON state.

Paragraph beginning at line 5 of page 28 has been amended as follows:

As described above, the optical signal of the n-th bit, the reference signal of the n-th bit, the optical signal of the (n+1)-th bit, and the reference signal of the (n+1)-th bit are outputted in this order through the output terminal VOUT of the common signal line 11. Then, the order of the optical signal and the reference signal is reversed from that in the photoelectric converter 1. However, similarly to the photoelectric converter according to the first embodiment of the present invention, a difference between the optical signal and the reference signal can be amplified in the signal processing circuit of FIG. 1 with the level VREF as a reference using the pulse signals ~~ÖSH1, ÖCLAMP, and ÖSH2~~ φSH1, φCLAMP, and φSH2 shown in FIG. 11.

Paragraph beginning at line 1 of page 35 has been amended as follows:

An operation of the photoelectric converter will hereinafter be described with reference to the timing chart shown in. FIG. ~~11~~ 16.

Paragraph beginning at line 3 of page 35 has been amended as follows:

~~ÖR, ÖRIN, ÖSIN, and ÖSEL~~ ϕR, ϕRIN, ϕSIN, and ϕSEL of FIG. 16 simultaneously operate for all bits. Since operation timings of ~~ÖS0, ÖR0, and ÖSCH~~ ϕS0, ϕR0, and ϕSCH vary depending on bits, ~~Ö80, ÖR0, and Ö8CH~~ ϕS0, ϕR0, and ϕSCH are denoted in the form of addition of "(n)".

Paragraph beginning at line 9 of page 35 has been amended as follows:

The transfer switch 15 is turned ON in accordance with a pulse S1 of ~~ÖSIN~~ ϕSIN to read out the optical signal obtained by storing electric charges generated due to incidence of light to the photodiode 1 to the capacitor 13. Next, at the time when the reset switch 2 is turned ON in accordance with a pulse R2 of ~~ÖR~~ ϕR, an output voltage appearing at an output terminal Vdi of the photodiode 1 is fixed to a reference voltage Vreset. On the other hand, at the time when the reset switch 2 is turned OFF, the output voltage appearing at the output terminal Vdi takes a value

which is obtained by adding an off-noise to the reference voltage Vreset. Here, the reference voltage Vreset is equal to the reference voltage VREF and has a small thermal noise, so that a fluctuation amount of a voltage of the terminal Vdi becomes smaller every time resetting is conducted.

Paragraph beginning at line 22 of page 35 has been amended as follows:

Next, right after the reset switch 2 is turned OFF, the transfer switch 14 is turned ON in accordance with a pulse R2 of ~~ÖRIN~~ $\underline{\phi RIN}$ to read out the reference signal after reset of the photodiode 1 to the capacitor 12. Thereafter, the photocharges are accumulated in the photodiode 1, and hence the electric potential appearing at the output terminal Vdi fluctuates in correspondence to a quantity of photocharges. Since a time interval for the storage ranges from a time point at which reading out of the pulse R2 of ~~ÖR~~ $\underline{\phi R}$ ends up to a time point at which reading out of the pulse S2 of ~~ÖSIN~~ $\underline{\phi SIN}$ of the next time interval ends, this time interval for the storage corresponds to a time interval TS2 shown in FIG. 6. Thus, this time interval for the storage is held for all bits.

Paragraph beginning at line 12 of page 36 has been amended as follows:

During a time interval TS2 for the storage shown in FIG. 16, if at the same time that the channel selection switch 7 is turned ON in accordance with a pulse of ~~ÖSCH(n)~~ φSCH(n), the transfer switch 17 is turned ON in accordance with a pulse of ~~ÖS0(n)~~ φS0(n), then an optical signal held in the capacitor 13 is read out to the common signal line 11. This time interval corresponds to a pulse width of a pulse S1 of ~~ÖSCH(n)~~ φSCH(n).

Paragraph beginning at line 19 of page 36 has been amended as follows:

This optical signal is a signal accumulated for a time interval TS1, and has as a reference a reset voltage that is reset by the pulse R1 of ~~ÖR~~ φR.

Paragraph beginning at line 22 of page 36 has been amended as follows:

Next, at the time when the transfer switch 16 is turned ON in accordance with a pulse of ~~ÖR0(n)~~ φR0(n), a reference signal held in the capacitor 12 is read out to the common signal line 11. This reference signal is a signal which is reset in accordance with a pulse R2 of ~~ÖR~~ φR.

Paragraph beginning at line 3 of page 37 has been amended as follows:

When a difference between the optical signal and the reference signal is taken in the signal processing circuit in a later stage, this results in that a difference between the reset levels of the different pulses of ~~ÖR~~ $\underline{\phi R}$ is taken. However, since thermal noises of the voltage Vreset are small, it is possible to take out only a voltage difference due to incidence of light.

Paragraph beginning at line 9 of page 37 has been amended as follows:

Next, if after ~~ÖSCH(n)~~ $\underline{\phi SCH(n)}$ is turned OFF, a channel selection switch 7 of the next bit is turned ON in accordance with ~~ÖSCH(n+1)~~ $\underline{\phi SCH(n+1)}$, and a transfer switch 17 of the next bit is turned ON in accordance with a pulse of ~~ÖS0(n+1)~~ $\underline{\phi S0(n+1)}$, then an operation for reading out an optical signal of the next bit is started. All other pulses of an (n+1)-th bit are shifted backwardly from the pulses of the n-th bit by a time interval when ~~ÖSCH~~ $\underline{\phi SCH(n+1)}$ is held in a turn-ON state.

Paragraph beginning at line 3 of page 38 has been amended as follows:

As described above, the optical signal of the n-th bit, the reference signal of the n-th bit, the optical signal of the (n+1)-th bit, and the reference signal of the (n+1)-th bit are outputted in this order through the output terminal VOUT of the common signal line 11. Then, the order of the optical signal and the reference signal is reversed from that in the photoelectric converter 1. However, similarly to the photoelectric converter according to the first embodiment of the present invention, a difference between the optical signal and the reference signal can be amplified in the signal processing circuit of FIG. 1 with the level VREF as a reference using the pulse signals ~~ÖSH1, ÖCLAMP, and ÖSH2~~ ϕSH1, ϕCLAMP, and ϕSH2 shown in FIG. 16.

Paragraph beginning at line 11 of page 41 has been amended as follows:

FIG. 18 is a schematic diagram of a close contact type image sensor according to a sixth embodiment of the present invention. A point of difference of this embodiment from the fourth embodiment is that in the inside of each image sensor IC 41, the reference voltage circuit 44 is provided, and also the resistor 45 is provided between the

output terminal of the reference voltage circuit 44 and the reference voltage terminal 46. A resistance value of the resistor 45 is set to about 1 ~~kΩ~~ KΩ.